Please amend the claims as follows. This listing of claims will replace all prior versions, and listings of claims in the application:

Listing of Claims:

Claim 1 (currently amended): A method for enhancing the fabrication process of a self-aligned contact (SAC) structure, the method comprising:

forming a transistor structure on a surface of a substrate;

forming a dielectric layer directly over the surface of the substrate without forming an etch stop layer thereon;

plasma etching a self-aligned contact hole through the dielectric layer in a plasma processing chamber;

monitoring a bias compensation voltage of the plasma processing chamber during the plasma etching; and

discontinuing the plasma etch process upon detecting an endpoint signaling change in the bias compensation voltage.

Claim 2 (currently amended): A method for enhancing the fabrication process of a self-aligned contact (SAC) structure as recited in claim 1, wherein the endpoint signaling change in the bias compensation voltage is detected when a portion of the surface of the substrate underlying the self-aligned contact hole is substantially exposed.

Claim 3 (original): A method for enhancing the fabrication process of a self-aligned contact (SAC) structure as recited in claim 1, wherein the endpoint signaling change is an expected step increase in the bias compensation voltage.

Claim 4 (original): A method for enhancing the fabrication process of a self-aligned contact (SAC) structure as recited in claim 1, wherein forming the transistor structure on the surface of the substrate includes,

forming a gate structure over the surface of the substrate;

forming spacers along sidewalls of the gate structure; and

forming source/drain diffusion regions into the surface of the substrate, the source/drain diffusion regions being defined substantially outside of the spacers formed along sidewalls of the gate structure.

Claim 5 (original): A method for enhancing the fabrication process of a self-aligned contact (SAC) structure as recited in claim 1, wherein the dielectric layer is an interlevel dielectric (ILD) layer.

Claim 6 (currently amended): A method for enhancing the fabrication process of a self-aligned contact (SAC), the method comprising:

forming a transistor structure on a substrate, the transistor structure including a gate structure formed over a first surface of the substrate;

forming spacers along sidewalls of the gate structure;

forming source/drain diffusion regions into the first surface of the substrate, the source/drain diffusion regions being defined substantially outside of the spacers formed along sidewalls of the gate structure;

forming an interlevel dielectric (ILD) layer directly over the first surface of the substrate without forming a stop layer, such that the ILD layer overlies the gate structure, the spacers, and the first surface of the substrate;

forming a contact hole and a via hole through the ILD layer implementing a plasma etching process such that the ~~contact~~ via hole is defined to a top layer of the gate structure and the ~~via~~ contact hole is defined to the source/drain diffusion regions;

monitoring an electrostatic chuck (ESC) bias compensation voltage during the plasma etching process; and

discontinuing the plasma etching process when an endpoint signaling change in the ESC bias compensation voltage is detected.

Claim 7 (currently amended): A method for enhancing the fabrication process of a self-aligned contact (SAC) as recited in claim 6, wherein the endpoint signaling change in the ESC bias compensation voltage is detected when a portion of the top layer of the gate structure underlying the ~~contact~~ via hole and a portion of the source/drain diffusion regions underlying the ~~via~~ contact hole are substantially exposed.

Claim 8 (original): A method for enhancing the fabrication process of a self-aligned contact (SAC) as recited in claim 6, wherein the gate structure includes,

a gate oxide formed over the first surface of the substrate; and

a polysilicon gate formed over the gate oxide.

Claim 9 (original): A method for enhancing the fabrication process of a self-aligned contact (SAC) as recited in claim 6, wherein forming the ILD layer over the first surface of the substrate includes,

depositing an oxide layer over the first surface of the substrate, the gate structure, and spacers;

depositing a tetraethylorthosilicate (TEOS) layer over the oxide layer; and

depositing an oxide layer over the TEOS layer.

Claim 10 (original): A method for enhancing the fabrication process of a self-aligned contact (SAC) as recited in claim 6, wherein forming spacers along the sidewalls of the gate structure includes,

depositing a spacer layer over a first surface of the substrate and the gate structure; and

performing a plasma etching process configured to define spacers along the sidewalls of the gate structure.

Claims 11-15 (cancelled)

Claim 16 (currently amended): A method for accurately detecting a plasma etch endpoint of a self-aligned contact (SAC), the method comprising:

providing a substrate having a transistor structure on a surface of the substrate;

forming a dielectric layer directly over the surface of the substrate without forming an etch stop layer thereon;

inserting the substrate into a plasma etching chamber so as to plasma etch a self-aligned contact hole through the dielectric layer;

introducing etchant gases into the plasma etching chamber;

powering up the plasma etching chamber, the powering up configured to strike a plasma so as to commence the plasma etching process;

monitoring a bias level of the plasma etching chamber during the plasma etching process; and

discontinuing the plasma etching process when an endpoint signaling change in a bias compensation voltage is detected.

Claim 17 (currently amended): A method for accurately detecting a plasma etch endpoint of a self-aligned contact (SAC) as recited in claim 16, wherein the endpoint signaling change in the bias compensation voltage is detected when a portion of the surface of the substrate underlying the self-aligned contact hole is substantially exposed.

Claim 18 (original): A method for accurately detecting a plasma etch endpoint of a self-aligned contact (SAC) as recited in claim 16, wherein the endpoint signaling change is an expected step increase in the bias compensation voltage.

Claim 19 (original): A method for accurately detecting a plasma etch endpoint of a self-aligned contact (SAC) as recited in claim 16, wherein the dielectric layer is an interlevel dielectric (ILD) layer.

Claim 20 (currently amended): A method for accurately detecting a plasma etch endpoint of a self-aligned contact (SAC) as recited in claim 17, wherein the portion of the surface of the substrate underlying the self-aligned contact hole is a gate structure.

Claim 21 (currently amended): A method for enhancing the fabrication process of a self-aligned contact (SAC) structure, the method comprising:

forming a transistor structure on a surface of a substrate;

forming a dielectric layer directly over the surface of the substrate without forming an etch stop layer thereon;

plasma etching a self-aligned contact hole through the dielectric layer in a plasma processing chamber;

monitoring a bias compensation voltage of the plasma processing chamber during the plasma etching; and

discontinuing the plasma etch process upon detecting an endpoint signaling change in the bias compensation voltage,

wherein the endpoint signaling change in the bias compensation voltage is detected when a portion of the surface of the substrate underlying the self-aligned contact hole is substantially exposed.

Claim 22 (previously presented): A method as recited in claim 21, wherein the bias compensation voltage is an electrostatic chuck (ESC) bias compensation voltage.

Claim 23 (previously presented): A method as recited in claim 1, wherein the bias compensation voltage is an electrostatic chuck (ESC) bias compensation voltage.

Claim 24 (previously presented): A method as recited in claim 16, wherein the bias compensation voltage is an electrostatic chuck (ESC) bias compensation voltage.